AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph bridging pages 30 and 31 to read as follows:

[0044] The electrode layers 31 and the metal layer 5 preferably cover not less than 80% of the area of the region 21a. Thus, the electrode layers 31 and the metal layer 5 sufficiently function as the light blocking layer. However, the electrode layers 31 should be spaced from each other, and the metal layer 5 should be spaced from the electrode layers 31. Therefore, the gaps g are inevitably present between the metal layer 5 and the respective electrode layers 31, making it impossible to cover 100% of the area of the region 21a or the entire region 21a with the electrode layers 31 and the metal layer 5. In order to provide sufficient gaps g between the respective electrode layers 31 and the metal layer 5 for prevention of short circuit between the electrode layers 31, the electrode layers 31 and the metal layer 5 preferably cover not more than 95% of the area of the region 21a. Alternatively, the electrode layers 31 may be formed as having a greater total area to cover 80 to 95% of the area of the region 21a without the provision of the metal layer 5.

Please amend the paragraph bridging pages 34 and 35 to read as follows:

[0050] Pattern formation of the electrode layers 31, 32 and the metal layers 5 on the collective substrate 1 may be achieved, for example, by forming a metal mask or a photolithographic mask and selectively metallizing exposed surface portions of the collective substrate 1 uncovered with the mask by the wet plating method or the physical vapor deposition. For the formation of the electrode layers 31, 32 of the multi-layer structure, the exposed surface portions of the ~~insulative members~~ collective substrate 1 are repeatedly metallized by employing different metals. When the electrode layers 31 and the metal layers 5 are formed on the main surface 21 and/or when the electrode layers 32 are formed on the external connection surface 22, the formation of the electrically conductive layers 33 is achieved simultaneously with the formation of the electrode layers 31 and/or the formation of the electrode layers 32 so as to connect the electrically conductive layers 33 to the electrode layers 31 and/or the electrode layers 32 by uncovering the openings of the through-holes 11 with the mask.

Please amend the paragraph bridging pages 40 and 41 to read as follows:

[0059] The main surface 21 continuous to the first taper surface 11b forms an obtuse angle θ_1 therebetween, and the external connection surface 22 continuous to the second taper surface 11c forms an obtuse angle θ_2 therebetween. Therefore, when the electrode layers 31, 32 and the electrically conductive layer 33 are formed, for example, by physical vapor deposition, printing, plating or the like, separation and uneven thickness of the layers metallized on an edge defined by the ~~first~~ second taper surface 11b and the main surface 21 and on an edge defined by the first taper surface 11c and the external connection surface 22 are significantly suppressed. Therefore, the electrode layers 31, 32 can be assuredly connected to the electrically conductive layer 33 without a connection failure, whereby the reliability of the resulting light emitting diode component LE2 and the resulting light emitting diode LE3 can be improved.

Please amend the paragraph **[0063]** at page 43, to read as follows:

[0063] The sandblast method described above is preferably employed for forming the through-holes 11 each having the aforesaid shape in the planar collective substrate prepared by preliminary firing by the post processing. In this method, the opening diameter of the minimum size hole portion 11a and the position of the minimum size hole portion 11a with respect to the thicknesswise of the insulative member ~~1~~ 2 can be arbitrarily controlled by adjusting the sandblasting depth and the sandblasting diameter for the formation of the taper surfaces 11b, 11c.

Please amend the paragraph bridging pages 56 and 57 to read as follows:

[0087] The area of the semiconductor element mount BL, i.e., the area of the main surface 21 or the external connection surface 22 of the insulative member 2 in this embodiment, is preferably 1.1 to 4 times the area of the light emitting element LE1 mounted on the main surface 21 (a projection area on the main surface 21). If the area of the semiconductor element mount BL is more than 4 times the area of the light emitting element LE1, it may be impossible to reduce the outer size for space saving. This makes it

impossible to handle the light emitting diode component ~~BL2~~ LE2 produced by mounting the light emitting element LE1 on the main surface 21 of the semiconductor element mount BL as a single component like the conventional light emitting element chip to incorporate the light emitting diode component BL2 in the package 7 for the light emitting diode LE3 or to mount the light emitting diode component BL2 on the board for the surface light emitting device. Further, the size of the semiconductor element mount BL is increased, so that a material loss caused when the light emitting element LE1 becomes defective is substantially the same as in the case of a conventional package.

Please amend the paragraph bridging pages 66 and 67 to read as follows:

[0107] The through-holes 11 preferably each have dimensions in substantially the same ranges as described above for the aforesaid reasons. Referring to Figs. 15 and 16, the position of the minimum size hole portion 11a with respect to the thicknesswise of the insulative member 2 is preferably such that a distance h between the main surface 21 and the minimum size hole portion 11a is more than zero and not more than 2/3 of the thickness t_0 of the insulative ~~member 1~~ member 2 , more preferably not more than 1/2 of the thickness t_0 of the insulative ~~member 1~~ member 2, further more preferably about 5μm to about 50μm. The opening width d of the minimum size hole portion 11a is preferably 10 to 200μm, more preferably 50 to 150μm, further more preferably 75 to 125μm. The term "opening width d" herein means a width of the elliptical shape which includes a rectangular center portion and semicircular portions respectively connected to opposite edges of the center portion, the width being measured perpendicularly to a center line extending through the centers of the semicircular portions.

Please amend the paragraph **[0108]** at page 67, to read as follows:

[0108] The thickness t_1 of a portion of the electrically conductive material 33a at the minimum size hole portion 11a as measured thicknesswise of the insulative member 2 is preferably 1/50 to 1/2, more preferably 1/20 to 1/5 of the thickness t_0 of the insulative ~~member 1~~ member 2. The thickness t_2 of the electrically conductive layer 33 provided on

the interior surface of the through-hole 11 is preferably 0.2 to 1.0 time, more preferably 0.3 to 0.5 times the opening width d of the minimum size hole portion 11a.

Please amend the paragraph bridging pages 71 and 72 to read as follows:

[0117] The two first taper surfaces 11b each have a cone-like taper shape having an opening diameter progressively decreasing from a main surface ~~21a~~ 21 of the insulative member 2 (on an upper side in the Figure) to the minimum size hole portion 11a of a round plane shape, and each have a round opening in the main surface 21 in the region 1a. The second taper surface 11c is tapered as having an elliptical plane shape including a rectangular center portion and semicircular portions provided on opposite edges of the center portion concentrically with the two minimum size hole portions 11a, and having a previously defined opening width progressively decreasing from the external connection surface 22 of the insulative member 2 (on a lower side in the Figure) to the two minimum size hole portions 11a, and has an elliptical opening in the external connection surface 22 across a region 1b between the two regions 1a.